Acta Technica *62* (2017), No. 7A, 299–310

Algorithm for removing baseline drift of filter signals based on singular value decomposition

Hailong Du[1], Zong Du[2], Chaofan Dai[3]

Abstract. In order to meet the needs of laboratory teaching and research, based on phase-locked loop technology designed a secondary radar signal generator, to achieve the 700MHz-1100MHz range of frequency synthesis. Firstly, the principle of frequency synthesis of phase-locked loop is analyzed, and the third-order passive loop filter is designed and realized. The high-frequency components generated by phase detector are filtered out and the phase-locked loop control circuit is formed with phase-locked loop chip ADF4350. Secondly, using the simulation tool ADI simPLL, the phase-locked loop is simulated and the parameters of the loop filter and the simulation output are obtained. Finally, the secondary radar signal generator system is built and the system output is analyzed by SPSS software. The results show that the system deviation is less than 0.02MHz and the fixed deviation is in the range of 1GHz-1.1GHz band. After the compensation, system accuracy can be very well to meet the needs of laboratory teaching and research.

Key words. Secondary radar, Signal generator, Phase-locked loop, Frequency synthesis.

1. Introduction

With the rapid development of radio technology, signal generator has become a widely used instrument and equipment in scientific R&D institutions and laboratories, and has been widely applied in the fields of electronic communication automatic control and civil aviation [1]. The secondary radar signal generator is a frequency signal source with high accuracy and high stability, which is used to realize the communication between the ground ATC base station and the aircraft, and to obtain the

[1]Engineering Technical Training Center, Civil Aviation University of China, Tianjin, 300300, China

[2]Department of Maintenance Engineering, Eastern Aviation Technology co., LTD. Gansu branch, Lanzhou, 730314

[3]Sino-European Institute of Aviation Engineering, Civil Aviation University of China, Tianjin, 300300, China

aircraft information of height and number and so on. As the electronic technology rapidly develops, the frequency synthesis technology can not only generate high stable frequency source, but can also meet the needs of frequent replacement frequency in the industry and research. Therefore, to generate a satisfactory signal source through the frequency synthesis technology is the core of the whole system design [2-4]. The frequency synthesis method of phase-locked loop (PLL) is an important method in frequency synthesis technique. Literature [5] employs the direct simulation frequency synthesis technology, which is fast in frequency conversion and with low phase noise, however, the largely use of frequency mixing, division, doubling and aluminum foil lead to its high cost, complex structure and uncontrollable spurious components. Literatures [6, 7] adopt direct digital frequency synthesis method, carries out frequency synthesis from the probability of the phase, which could get different frequencies as well as random waveform signals. However, the noise brought by the spurious frequency through the non-ideal filter would increase with the increase of frequency, which makes this method not applicable to the synthesizers with high synthesis frequency. Literatures [8, 9] use the indirect method to synthesize the frequency through phase lock loop (PLL) technology, although the frequency conversion time is longer, for a system with ordinary requirements on this issue, this method has high output resolution, good restrain effect on spurious signals, and low phase noise, besides, its output frequency can meet the requirements of frequency source raised by secondary radar. Therefore, the phase lock loop (PLL) frequency synthesis technology can be used in the manufacture of the frequency generator in the secondary radar.

2. The principle of phase lock loop (PLL) frequency synthesis

As shown in Figure 1, the phase locked loop is mainly composed of voltage-controlled oscillator (VCO), phase detector (PD), low pass filter (LPF) and referential frequency source (crystal oscillator) [9-11].

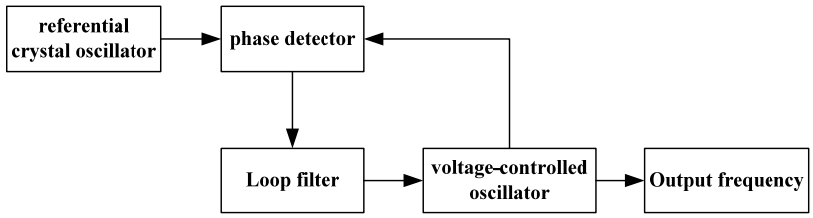


Fig. 1. The basic block diagram of phase lock loop

Phase detector is also called the phase comparator, as an important part of the phase-locked loop circuit; its function is to detect the phase difference between the input signal and output signal, to convert the detected phase difference into the voltage signal for output, and to form the control voltage of the VCO after the output voltage of the phase detector after passing the low pass filter. The phase

detector mainly adopts the sine wave phase detector and pulse sampling preserving phase comparator. Comparing with the sine wave phase detector, the pulse sampling preserving phase comparator used in this paper has low output ripple voltage and pure final loop output spectrum; therefore, it is usually used in the digital phase-locked loop. In the phase-locked loop, the loop filter is essentially a low pass filter, which is a linear circuit composed of capacitance and resistance. On the one hand, it could filter and remove the high frequency component and output ripple generated by the phase detector, limit the out-of-band noise, and extract the average component to control the frequency of the VCO; on the other hand, the loop filter is also an important parameter adjusting device in the PLL, the size of the pull-in range, pull-in time, tracking time, loop stability and noise label, etc. can be changed by altering the parameters of the loop filter. Therefore, the loop filter will directly affect the phase noise and spectrum purity of the output frequency. The common filters used in the phase lock loop are passive RC filter, active proportion integration filter, and so on [4].

Voltage-controlled oscillator is the device that converts voltage to frequency. Within the output range, there is a corresponding function relationship between the output signal and the control voltage. However, the change of its output signal frequency and the input signal voltage change are linear in a limited range, while its control sensitivity will decrease beyond this range. The relationship between oscillation frequency ω_v and control voltage is shown in Figure 2:

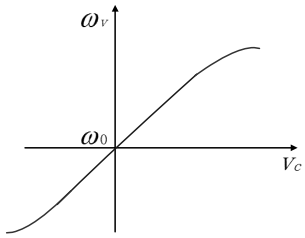


Fig. 2. The characteristic curve of the voltage-controlled oscillator

ω_0 is the inherent frequency of the voltage-controlled oscillator with no control voltage input, it can be seen from FIG. 2 that the curve can be approximately straight in the vicinity of the inherent frequency, and there is a linear relation between ω_v and v_c, which could be expressed by the following equation:

$$\omega_v(t) = \omega 0 + K_v V_c(t)\,. \tag{1}$$

The slope K_v of the straight line part can be fitted out to indicate the changing amplitude of the output frequency in the voltage controlled oscillator with the control voltage.

From the relations between the instantaneous frequency $\omega(t)$ and phase $\theta(t)$:

$$\omega(t) = \frac{d\theta(t)}{dt} \tag{2}$$

Then

$$\theta(t) = \int \omega(t)dt + \theta_0 \ . \tag{3}$$

In this formula, θ_0 is the initial phase. When the output frequency of VCO and crystal oscillator is added to that of the phase detector, the frequency difference between the two oscillation signals is:

$$\Delta\omega(t) = \omega_R - \omega_V \ . \tag{4}$$

Where, ω_R is the fixed-frequency of the referential crystal oscillator, ω_V is the output frequency of the VCO. The instantaneous phase difference under this condition is:

$$\theta e(t) = \int \Delta\omega(t)dt + \theta_0 \, . \tag{5}$$

When $\omega_R = \omega_V$, and $\Delta\omega(t) = 0$:

$$\theta e(t) = \theta_0 \, . \tag{6}$$

According to Equation (6), when the output frequency of VCO is equal to the fixed frequency of the referential crystal oscillator, the instantaneous phase difference is a constant.

As shown in Figure 1, when the output frequency of the VCO changes, according to Equation (3), the phase difference between the input signals of the referential crystal oscillator and the output signals of the VCO is no longer a fixed value, which lead to the voltage change of the phase detector, and the output frequency of the VCO will also change, until

$$\omega_R = \omega_V \, . \tag{7}$$

When the Equation (7) is satisfied, the frequency of the phase-locked loop will be locked and output, and the output frequency is equal to the target input frequency at this time.

3. The system implementation of secondary radar signal generator

3.1. System composition

Figure 3 is the block diagram of the secondary radar signal generator system. During the process of system design and development, the designed secondary radar signal generator can act as the standard frequency source of the secondary radar as well as the radio frequency signal source or test equipment. This paper uses the phase-locked loop integrated circuit ADF4350 and loop filter to form the phase-lock loop to be the core of frequency synthesis, so that the system could has a wider frequency output; STM32F405RGT6 microcontroller is the core controller of the system to guarantee the good operation of the whole control system. The DWIN DGUS screen allows touch input, which makes it convenient to input the target

frequency and send the default frequency to the core controller.

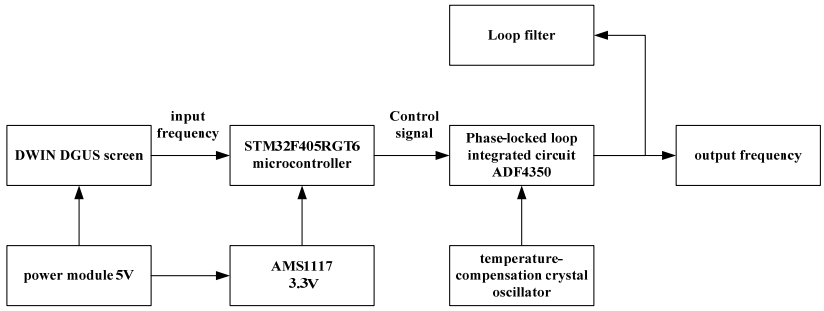


Fig. 3. The system composition

The phase-locked loop integrated circuit ADF4350 is a high performance chip with the fundamental wave frequency range of 2200MHz-4400MHz, which integrated the phase detector, voltage control oscillator, digital frequency divider and process control circuit. The frequency output of 108MHz-4.4GHz can be achieved through the internal frequency dividing circuit. Figure 4 below shows the build-in functions of the frequency synthesizing chip ADF4350.

As shown in Figure 4, the ADF4350 chip is able to realize integer and fractional frequency division. With the fractional frequency division function of ADF4350, the R and D values of the frequency divider can be determined when the input frequency of the frequency reference source is confirmed and the parameters of the external loop filter are set. Equation (8) and (9) shows the relationship between the output frequency *RFout* and the frequency of the phase detector *FPFD* and the referential input frequency *REFIN*, the integer frequency division factor *INT*, the numerator of the fractional frequency division *FRAC* and the denominator of the fractional frequency division *MOD* as follows:'

$$RF_{out} = [INT + (F_{RAC}/MOD)] * F_{PFD} \,. \tag{8}$$

$$f_{PFD} = REF_{IN} * [(1 + D) / (R * (1 + T))] \,. \tag{9}$$

There, T is the 2 bit frequency division of the referential input frequency(0 or 1)[13], D is the frequency division ratio of the binary decade programmable reference counter, R is the decade frequency divider with the frequency dividing ratio from 1 to 1023, which is used to generate the referential input frequency of the phase detector.

3.2. Loop filter design

The loop filter is a key part in the circuit design in the secondary radar signal generator. It is used to guarantee the passing of the difference frequency components output by the ADF4350 IC phase detector, filter and remove the high-frequency interference to get a stable loop and a better noise suppression effect[1415]. In

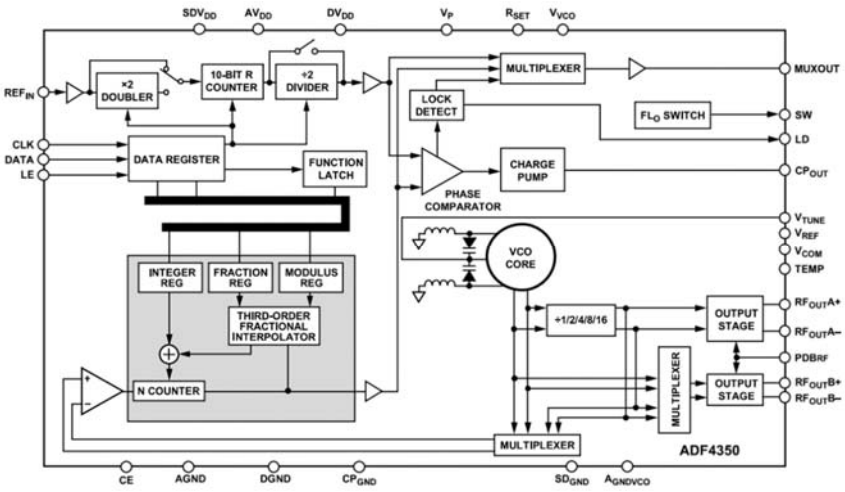


Fig. 4. The internal function of ADF4350 Although the phase-locked loop integrated circuit integrates the phase detector and the voltage-controlled oscillator, the lack of loop filter makes it essential to design a reasonable and reliable loop filter to from a complete phase locked control loop.

practice, the commonly used loop filters are mainly passive filter and active filter, and the latter one is composed of operational amplifier and several discrete components. Due to the high working frequency output by the secondary radar signal generator (with the design target between 700MHz-1100MHz), the ordinary active amplifier cannot work at such high frequency and will introduce additional noise. Therefore, during the circuit design of the loop filter, the third-order passive filter is selected as the loop filter [16]. Figure 5 shows the third-order passive filter designed in this paper.

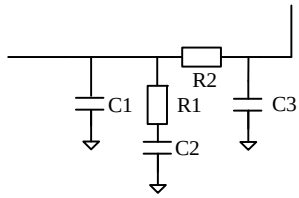


Fig. 5. The third-order passive loop filter

4. Parameters simulation

With the specialized design and simulation tools software ADI simPLL provided by ADI Company, the loop filter property simulation and the parameter design are accomplished; through the simulation of phase-locked loop model, the reference value of the third-order passive filter components could be got, which not only avoids the

tedious manual calculation, but also verify the loop bandwidth and phase margin of the loop filter. Connecting the ADF4350 circuit with the third-order passive loop filter designed in section 2.2, the peripheral circuit simulation diagram of the ADF4350 is completed as shown in Figure 6.

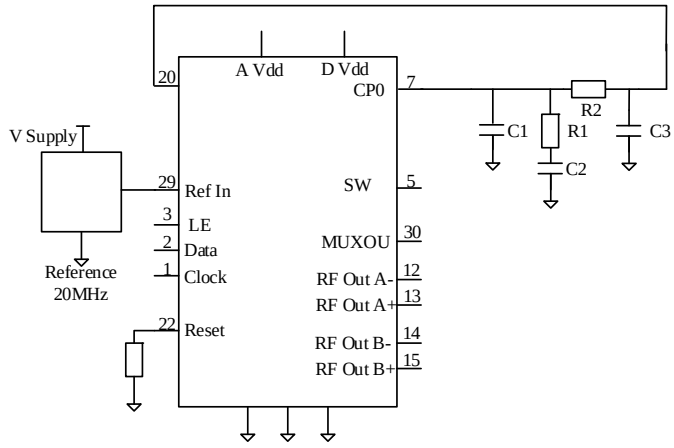


Fig. 6. Peripheral circuit simulation diagram of ADF4350

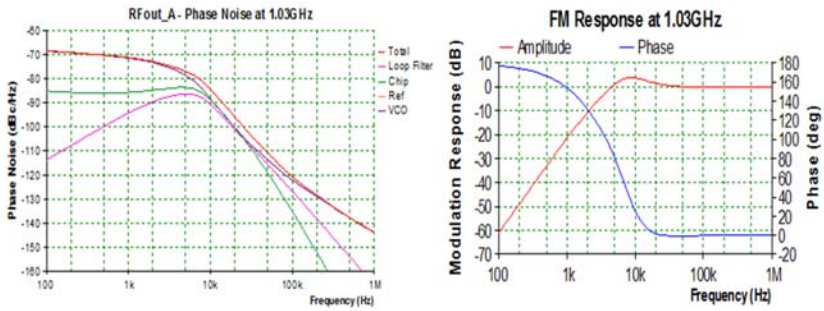
Setting the bandwidth of the loop as one tenth of the phase frequency, the output frequency within 700MHz -1100MHz, and the phase margin of 45 degrees, the circuit device parameters of the chip can be obtained by software simulation. The resistance value of *Reset* through simulation is 5.1kΩ, and the estimated loop current is 5Ma. Meanwhile, the simulation software also gives the recommended parameters of the loop filter, as shown in Table 1.

Table 1. The filter parameters

C1	C2	C3	R1	R2
2.55pF	40.7pF	1.37pF	11.0K	22.4K

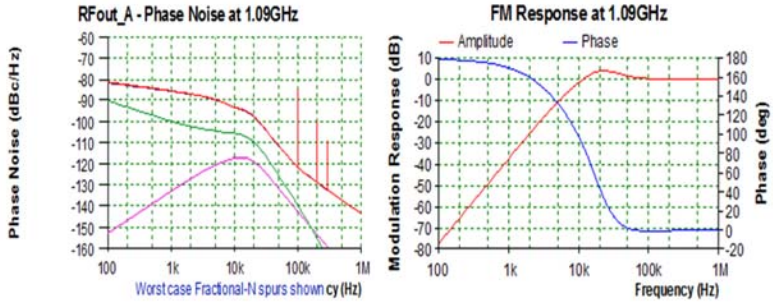
The simulation results of the system phase noise and filter property obtained by using this filter parameter are shown in Fig.7 and 8.

Figure 7 and Figure 8 shows that the system gets the biggest phase noise of 70dB and -80dB at the frequency of 1030 MHZ and 1090 MHZ; through filter property simulation diagram, it can be found that the phase margin at 1030 MHZ and 1090 MHZ are close to 45 degrees, and the amplitude margin is - 50 db. This indicates that the simulation system is stable, the phase noise has little influence on the output frequency, and the simulation results meet the requirements of system design.



(a) Phase noise simulation diagram (b) Filter property simulation diagram

Fig. 7. 1030MHz loop filter wave property simulation diagram



(a) Phase noise simulation diagram (b) Filter property simulation diagram

Fig. 8. 1090MHz loop filter wave property simulation diagram

5. System testing

In order to verify the actual output performance of the system, the paper tests the stability of signal frequency, the output bandwidth, and the clutter index around the signal frequency source. With the scanning bandwidth set at 100MHz, the system output is tested by DSA1030 frequency spectrograph to observe the clutter and the frequency stability. The frequency test range is 700MHz-1100MHz, and the transmitting frequency of 1030MHz and the received frequency of 1090MHz of the secondary radar are also tested. Some results of the random test with the radio-frequency band of 1GHz-1.1GHz is shown in Table 2.

Using SPSS software to conduct statistic analysis on the data in the above tables, it can be seen that when the scanning bandwidth of the frequency spectrograph is set at 100MHz, within the frequency ban range of 1GHz-1.1GHz, there is certain deviation between the output frequency and the target input frequency of each frequency point, but the deviation is a fixed frequency difference of 0.0167MHz rather than the deviation of the output frequency caused by the unstable output frequency of the peripheral reference crystal oscillator. Therefore, the input process of the system can be compensated to achieve a higher precision. After testing, the

minimum output frequency of the system is obtained as 519MHz, while the maximum output frequency is 1140MHz.

Table 2. System output bandwidth measurement

Random frequency	actual output(MHz)	output power (dBm)
1001.3	1001.2833	8.13
1002.0	1001.0833	8.13
1002.6	1002.5833	8.10
1004.8	1004.7833	8.05
1007.5	1007.4833	7.97
1035.4	1035.3833	6.86
1037.8	1037.7833	6.74
1042.1	1042.0833	6.56
1028.9	1028.8333	7.14
1019.5	1019.4833	7.55
1048.7	1048.6833	6.25
1055.4	1055.3833	5.93
1065.4	1065.3833	5.45
1079.4	1079.3833	4.72
1081.2	1081.1833	4.50
1085.6	1085.5833	4.32
1090.5	1090.4833	3.95
1098.7	1098.6833	3.24

When inputs 1030MHz and 1090MHz in the system respectively and makes compensation on the basis of the fixed deviation, the observed output frequency as shown in Fig. 9 and Fig. 10. From the figures it can be found that after compensation, the system could accurate response to the input frequency values and the power of the spurious noise is much lower than the target frequency, which could successfully meet the design requirements of the system.

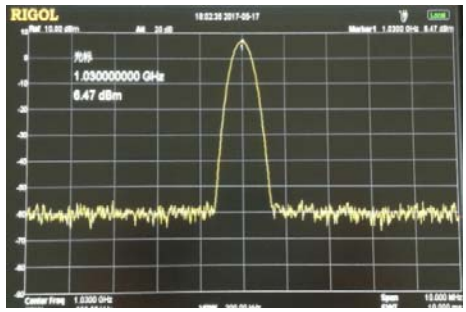


Fig. 9. 1030MHz frequency output

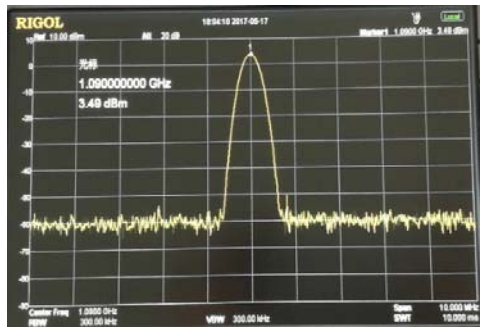


Fig. 10. 1090MHz frequency output

6. Conclusions

This paper designs a secondary radar signal generator on the basis of phase-locked loop technology, which realizes the frequency synthesis within the range of 700MHz-1100MHz. Furthermore, the three-order passive loop filter is designed and forms the phase locked loop control loop with the ADF4350phase-locked loop IC. With the simulation software ADI simPLL, the phase locked loop is simulated, and the parameters and simulation output features of the loop filter are obtained. Using SPSS software to analyze the sampling results shows that the system deviation within frequency band between 1GHz to 1.1GHz is a fixed deviation less than 0.02 MHz, also the precision after compensation could perfectly meet the requirements of teaching and research in the laboratory.

References

[1] G. Blasco, E. Isern, E. Martin: *Design of a stable pulse generator system based on a Ring-VCO Phase-Locked Loop using 180nm CMOS technology*[C]// Design of Circuits and Integrated Systems. IEEE, (2016), 1–6.

[2] H. E. Jiai, X. Chen: *Design of phase-locked loop frequency synthesizer based on CDCE913*[J]. Modern Electronics Technique, (2016).

[3] H. E. Jiai, X. Chen X.: *Design of phase-locked loop frequency synthesizer based on CDCE913*[J]. Modern Electronics Technique, (2016).

[4] B. Jiang , W. Sheng, R. Zhang, et al.: *Adaptive angle tracking loop design based on digital phase-locked loop*[J]. Signal Processing, *125* (2016), No. C, 221–236.

[5] H. B. Chen, J. Y. Min: *Research on Single-phase Phase-locked Loop Based on Orthogonal Signal Generator*[J]. Power Electronics (2014).

[6] L. I. Wei-Feng, Z. Wang Z.: *Design of Single-phase Digital Phase-locked Loop Based on Double Park Transformation*[J]. Journal of Zhongyuan University of Technology, (2015).

[7] N. Zhang: *Design of All Digital Phase-locked Loop Based on FPGA*[J]. Journal of Changchun University of Science & Technology, (2016).

[8] L. I. Peng: *Design and Realization of An Integer/Half-integer Frequency Synthesizer Based on Phase-locked Loop Technology*[J]. Shipboard Electronic Countermeasure, (2014).

[9] C. Zhang, D. Yang, L. I. En, et al.: *Design of Digital Phase-locked Loop of Induction Heating Based on TMS320F28335*[J]. Hot Working Technology, (2016).

[10] W. U. Linyong, L. I. Chunlin: *A Design of Multi-channel Synchronized Radar-Echo-Signal Generator Based on AD9959*[J]. Electronic Science & Technology, (2014).

[11] M. Keaveney, P. Walsh: *Phase locked loop (PLL) based frequency sweep generator: US*, US 8638139 B2[P], (2014).

[12] L. Zhai: *Design and Implementation of Radar Signal Generator Based on SOPC*[J]. Henan Science, (2016).

[13] Q. Y. Kou, L. Zhang, X. Q. Zhang, et al.: *Design of Radar Signal Generator Based on CPLD*[J]. Journal of Astronautic Metrology & Measurement, (2014).

[14] Q. Gao, M. Li, X. University: *Design of Signal Generator Based on AD9852 for Ground Test Equipment*[J]. Fire Control Radar Technology, (2014).

[15] Q. Wang, Y. Bai, B. Zhu, et al.: *A new design of seed source used in optical streak camera*[J]. Hongwai Yu Jiguang Gongcheng/infrared & Laser Engineering, *44* (2015), No. 7, 2122–2126.

[16] H. Paik, N. N. Sastry, I. Santiprabha: *Estimation of break-lock in PLL synthesizers for monopulse radar applications: Experimental and simulation approach*[J]. Engineering Science & Technology An International Journal, *19* (2016), No. 1, 22–30.

Received May 7, 2017